10-16-00 A

Jc535 U.S. PTO 10/12/00

Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (4/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	00-285
First Inventor or Application Identifier	Feng Qian
Title	Frame Matching Method
Express Mail Label No.	EL715231755US

Jc806 U.S. PTO 09/687700 10/12/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* (Submit an original and a duplicate for fee processing)
2. [X] Specification [Total Pages 10] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 2]
4. Oath or Declaration [Total Pages 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: .....

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No. _____/_____
Prior application information: Examiner _____ *Group / Art Unit:* _____
For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* (Insert Customer No. or Attach bar code label here) or [ ] *Correspondence address below*

Name					
Address					
City		State		Zip Code	
Country		Telephone		Fax	

Name (Print/Type)	Sandeep Jaggi	Registration No. (Attorney/Agent)	43,331
Signature		Date	10-12-00

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Feng Qian

For : Frame Matching Method

§

I hereby certify that this correspondence is being deposited with the U.S Postal Service as Express Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington D C 20231, on the date indicated below

Manu Kashyap

Date 10/12/00 Signature

Atty Docket : 00-285

TRANSMITTAL LETTER FOR PATENT APPLICATION

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir,

The following paper(s) and/or fee(s) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee", addressed to :

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

1. Fee Transmittal Form (in duplicate).
2. Patent Application comprising the following :

   a. Specification, pages = 10

   b. Drawing, sheets = 2

   c. Assignment and declaration with power of attorney.

It is respectfully requested that the Commissioner accord the enclosed patent application a filing date and a serial number.

If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 12-2252.

Respectfully submitted,

Sandeep Jaggi

Reg. No. 43,331

LSI Logic Corporation
1551 McCarthy Blvd., MS D-106
Milpitas, CA 95035
408/433-7475

Date: 10-12-2000

PTO/SB/17 (12/99)
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FEE TRANSMITTAL for FY 2000

Patent fees are subject to annual revision.
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12. See 37 C.F.R. §§ 1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT ($) 690.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Feng Qian
Examiner Name	
Group / Art Unit	
Attorney Docket No.	00-285

METHOD OF PAYMENT (check one)

1. [x] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 12-2252

Deposit Account Name: LSI Logic Corporation

[x] Charge Any Additional Fee Required Under 37 CFR §§ 1.16 and 1.17

2. [ ] **Payment Enclosed:** [ ] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	690
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 690.00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below		Fee Paid
Total Claims	6	-20** =		X =	0
Independent Claims	1	- 3** =		X =	0
Multiple Dependent				=	

***or number previously paid, if greater; For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	190	Extension for reply within second month	
117	870	217	435	Extension for reply within third month	
118	1,360	218	680	Extension for reply within fourth month	
128	1,850	228	925	Extension for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	690	246	345	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	690	249	345	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 0

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Sandeep Jaggi	Registration No. (Attorney/Agent)	43,331	Telephone	408/954-4923
Signature				Date	10-12-00

WARNING:

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PATENT

Docket: 00-285

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MANU KASHYAP
[NAME OF PARALEGAL]

Frame Matching Method

By:

Feng Qian
25851 Majorca Way
Mission Viejo, CA 92692
Citizenship: U.S.

09685704 - 101200

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to frame based digital communication systems and more particularly to a method for processing frames having a certain size in systems configured for frames having a different size.

Description of the Related Art

Digital data is often communicated in frames, which are groups of digital data that are processed together, as will be further described below. Often, it is desired to send or receive frames having a certain size in systems configured for different sized frames. For example, in the IS2000.2-A standard for code division multiple access (CDMA) communications, encoded symbols at a rate of L symbols per frame must be matched with a transmission scheme that processes N symbols per frame, where N is greater than L. In this case, for any one frame, the L symbols are repeated M times, where M is the smallest integer such that ML>N. Then, the ML symbols are reduced to N symbols by deleting (puncturing) P symbols, where P= ML-N. There is no appreciable loss of information since in CDMA, many symbols are redundant to provide robust protection against transmission errors; deleting a few redundant symbols will typically not cause any significant problems, especially if the symbols are far apart.

The above mentioned two stage approach has drawbacks. If complex control logic is not used, then it requires unnecessary additional memory to store the ML symbols; in the worst case, this can be almost twice as much memory as would otherwise be required if the actual frame size is only 1 bit shorter than the standard frame size. Moreover, additional data transfer (re-arrangement) is needed because of the two-stage processing.

It would be desirable to improve upon the above mentioned scheme.

SUMMARY OF THE INVENTION

According to the present invention, a frame of digital data with L symbols is matched to a frame with N symbols without (preferably) the need for performing any puncturing. This is performed by making that number of copies of the original L symbols that results in N symbols. In particular, M=floor(N/L) is computed. L2=N-ML is computed. (L1=L-L2 where L1 and L2 solve the simultaneous equations L1+L2=L and L1*M+L2*(M+1)=N). The frame is effectively divided into two mutually exclusive groups of symbols; one group (consisting of L1 symbols) is copied M times and the other group (consisting of L2 symbols) is copied M+1 times.

Docket No. 95-0

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Figure 1 is a block diagram of a possible digital communication system that includes a frame matching circuit the implements a frame matching method according to the present invention.

Figure 2 is a flow chart of a frame matching method according to the present invention.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

This specification describes frame matching methods in the context of CDMA systems. However, it will be appreciated that the present invention is not restricted to CDMA systems.

Figure 1 represents a digital communications system 140 within which the present invention may be embodied. As shown, the digital system 140 comprises a discrete-time channel 142 interposed between an encoder 144 and a decoder 130. Discrete-time channel 142 comprises a modulator 146, a channel 148 and a demodulator 150. An interleaver 145 is interposed between the encoder 144 and the modulator 146. A deinterleaver 151 is interposed between the decoder 130 and the demodulator 150. Channel 148 may be a transmission channel or a storage medium being written to and read from. Interleaver 145 receives a digital output signal from a rate matching circuit 147, which in turn receives a digital signal from an encoder 144. The interleaver 145 interleaves this digital output signal over a certain time period, which is usually predetermined and known as a frame. Modulator 146 serves to translate the digital output signal from interleaver 145 into signals suitable for channel 148 and thereafter drives the signals across channel 148.

Channel 148 may suffer from interference that corrupts said signals, the interference possibly taking form in any combination of additive noise, cross channel interference, multi-path interference, and channel fading. Demodulator 150 serves to receive the signals from channel 148 while minimizing the interference as much as is practical, and thereafter translate the signals into digital signals for input to deinterleaver 151, which deinterleaves the digital signal and provides it to decoder 130. Discrete-time channel 142 can thus be viewed as a unit accepting digital input signals and producing

possibly corrupted digital output signals although the present invention is not limited to noisy channels.

Encoder 144 is a convolutional encoder which serves to add redundancy to input data signal 152. The output of the encoder 144 is L symbols per frame, which must be matched with the interleaver 145, which interleaves N symbols per frame, where N is greater than L. This matching is performed by the rate matching circuit 147, which repeats the L symbols of an input frame in such a manner that an N symbol frame is produced.

Figure 2 is a flow chart that describes an embodiment of the matching circuit 147 according to the present invention. In block 198, a frame is received. (It will be appreciated that the frame need not be received all at once and the steps described below may be initiated before the entire frame is received). In block 200, M=floor(N/L) is computed. In block 202, L2=N-ML is computed. (L1=L-L2 where L1 and L2 solve the simultaneous equations L1+L2=L and L1*M+L2*(M+1)=N). As will be described further below, the frame is effectively divided into two mutually exclusive groups of symbols; one group (consisting of L1 symbols) will be copied M times and the other group (consisting of L2 symbols) will be copied M+1 times.

The below described steps serially process the symbols, selecting each symbol for inclusion in one group or the other. It will be appreciated that the two groups may be distributed in any manner so long as the totals for each group are L1 and L2 respectively at the end of the frame. For example, the first L1 symbols in a frame could be selected for the first group and the remaining L2 symbols selected for the second group. According to the preferred embodiment described below, the distribution is such that, at any time in the process, the ratio between A/B is as close to 1 as possible, where A is the total number of symbols that have previously been selected for the first group and B is the

total number of symbols that have previously been selected for the second group. In other words, the groups are selected more or less evenly, according to the ratio L1:L2.

In block 204, two variables, SymbolCnt and RatioCnt are initialized to 0. Block 206 is the start of a while loop, which exits at block 220 (and is then further processed by a digital communications system, which, in the case of the system in Figure 1, means it is then interleaved by interleaver 145) when SymbolCnt is equal to L (i.e. it exits when all of the symbols have been processed). Within the while loop, an array NumberOfRepeat is indexed by SymbolCnt; each element in NumberOfRepeat stores the number of times the symbol corresponding SymbolCnt will be multiplied (i.e. either M or M+1 times). For example, if NumberOfRepeat(0) = M, then the 0^{th} symbol will be repeated M times. Specifically, in block 208,, NumberOfRepeat(SymbolCnt) is set equal to M.

In block 210, a variable RatioCnt is set equal to its current value + L2. RatioCnt, as its name implies, essentially tracks the distribution between multiplications by L1 and L2. In block 212, it is determined whether RatioCnt is greater than or equal to L. If so, this means that the current symbol must be repeated M+1 times; thus, in block 214, NumbeOfRepeat(SymbolCnt) is set to M+1 (i.e. its current value M, incremented by 1). Also, RatioCnt must be reduced by L, which is done in block 216. In block 218, SymbolCnt is incremented and the process loops back to block 206.

Conclusion

Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the following claims be interpreted to embrace all such variations and modifications.

WHAT IS CLAIMED IS:

1. A method for increasing the size of a frame of digital data from a first number of original symbols (L) to a second number of symbols (N), where the digital data comprising the frame is ordered from a first bit to an Lth symbol, the method comprising the steps of:

(a) Receiving the frame;

(b) Storing in a digital memory a first integer number (M) of copies of each of a first group of the original symbols, where M is greater than 1;

(c) Storing in the digital memory at least one copy of each of a second group of the original symbols;

(d) Further processing the symbols stored in the digital memory according to steps (b) and (c) in a digital communications system;

wherein the frame consists of the first group and the second group and the first group and the second group are mutually exclusive; and wherein

steps (b) and (c) are performed such that the total number of symbols copied to the digital memory in steps (b) and (c) is equal to N.

2. The method according to claim 1 wherein step (b) is performed such that each of the second group of symbols is multiplied by the same number X.

3. The method according to claim 2 wherein X = M+1.

4. The method according to claim 3 wherein the first group and the second group are selected by serially processing the symbols.

5. The method according to claim 4 wherein symbols are selected to be in the first group or the second group such that the ratio between A/B is as close to 1 as possible, where A is

the total number of symbols that have previously been selected for the first group and B is the total number of symbols that have previously been selected for the second group.

6. The method according to claim 1 wherein M=floor(N/L).

Document ID: 2004/0202249

ABSTRACT OF THE DISCLOSURE

A frame of digital data with L symbols is matched to a frame with N symbols by making that number of copies of the original L symbols that results in N symbols. In particular, M=floor(N/L) is computed. L2=N-ML is computed. (L1=L-L2 where L1 and L2 solve the simultaneous equations L1+L2=L and L1*M+L2*(M+1)=N). The frame is effectively divided into two mutually exclusive groups of symbols; one group (consisting of L1 symbols) is copied M times and the other group (consisting of L2 symbols) is copied M+1 times.

Docket No. 50277-2350

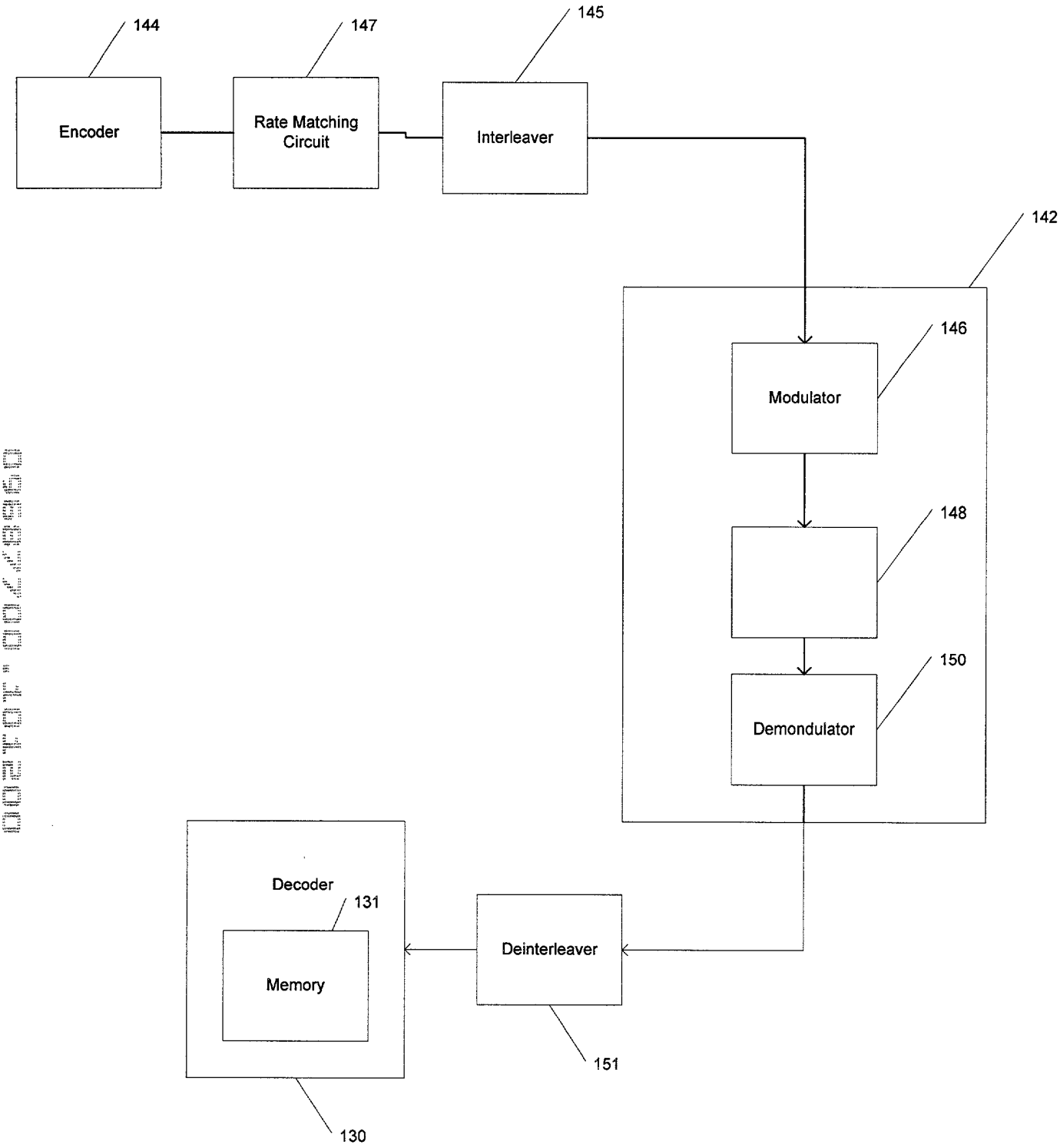
144
147
145
Encoder
Rate Matching Circuit
Interleaver
142
146
Modulator
148
150
Demondulator
Decoder
131
Memory
Deinterleaver
151
130

Figure 1

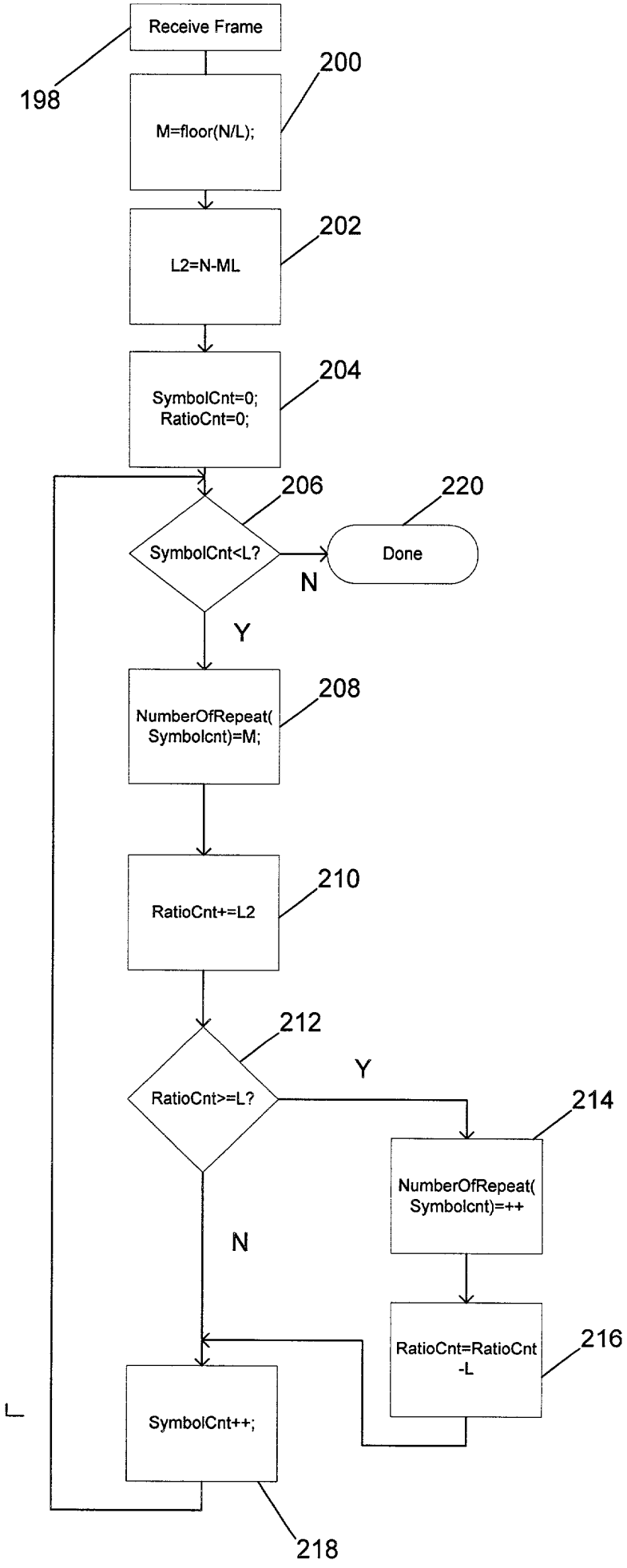
Receive Frame
198
200
M=floor(N/L);
202
L2=N-ML
204
SymbolCnt=0;
RatioCnt=0;
206
220
SymbolCnt<L?
Done
N
Y
208
NumberOfRepeat(
SymbolCnt)=M;
210
RatioCnt+=L2
212
Y
RatioCnt>=L?
214
NumberOfRepeat(
SymbolCnt)=++
N
216
RatioCnt=RatioCnt
-L
SymbolCnt++;
218

Figure 2

Declaration, Power of Attorney, Correspondence Address, and Petition

Docket Number : 00-285

Declaration

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first, and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Single Stage Variable Data Repetition Scheme for Frame Matching

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Power of Attorney

I hereby appoint David G. Pursel, Reg. 28,659; Ralph R. Veseli, Reg. 33,807; Bruce R. Hopenfeld, Reg. 39,714; Gary Edward Ross, Reg. 29,431; Lloyd E. Dakin, Reg. 38,423; and Sandeep Jaggi, Reg. 43,331; as my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith and before competent international authorities.

Correspondence Address

Please send all correspondence to:

LSI Logic Corporation
Corporate Legal Department
Intellectual Property Services Group
1551 McCarthy Blvd., M/S D-106
Milpitas, CA 95035
Phone: (408) 433-8708
Fax: (408) 433-7770

Petition

Wherefore I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, and I hereby subscribe my name to the foregoing specification and claims, declaration, power of attorney, and this petition.

Declaration, Power of Attorney, Correspondence Address, and Petition

First named inventor

First Name Feng **Last Name:** Qian

Inventor's Signature: **Date** 8/14/2000

Address 25851 Majorca Way

City Mission Viejo CA 92692 United States

Citizenship United States

DOCKET NO. 20020.0